UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/727,811	12/04/2003	Gheorghe Stefan	5227-01-2	7461

7590 10/31/2006

Nicholas J. Tuccillo, Esq.
McCormick, Paulding & Huber LLP
CityPlace II
185 Asylum Street
Hartford, CT 06103

EXAMINER	
GEIB, BENJAMIN P	

ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 10/31/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/727,811	STEFAN ET AL.	
	Examiner	Art Unit	
	Benjamin P. Geib	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-82* is/are pending in the application.

4a) Of the above claim(s) *1-21* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *22-25,28,30-34,38,43,44,47,51,52,59 and 78-82* is/are rejected.

7)☒ Claim(s) *26,27,29,35-37,39-42,45,46,48-50,53-58 and 60-77* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

FRITZ FLEMING
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100
10/27/2006

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *06/21/2004, 01/09/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 22-82 have been examined.

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Application on 12/04/2003, Information Disclosure Statement on 06/21/2004, Information Disclosure Statement on 01/09/2006, Request for status of Application on 06/12/2006, and Response to Restriction on 07/21/2006.

Election/Restrictions

3. Claim 1-21 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 07/21/2006.

Claim Objections

4. Claims 33 and 34 are objected to because of the following informalities:

Regarding claim 33, the phrase "wherein said 'find' command" at line 5 of the claim should be changed to "wherein said 'find and mark left' command".

Regarding claim 34, the phrase "wherein said 'match' command" at line 5 of the claim should be changed to "wherein said 'match and mark left' command".

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claim 80 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7. Regarding claim 80, the claim recites the phrase "said key field" at lines 3 and 5 of the claim. This phrase renders the claim indefinite as it is unclear which one of the two previously mentioned key fields (i.e. "variable-length key field" and "key field") is being referred to.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 22-25, 28, 30-34, 38, 43, 44, 47, 51, 52, 59, and 78-82 are rejected under 35 U.S.C. 102(e) as being anticipated by Stefan et al., U.S. Patent No. 6,760,821 (Herein referred to as Stefan).

10. Referring to claim 22, Stefan has taught a data processing system, said data processing system comprising:

an associative memory device *[connex memory; Fig. 2, component 206]* containing n-cells *[column 4, lines 20-41]*, each of said n-cells including a processing circuit *[comparator; Fig. 14, component 55]* and m-bits of memory capacity *[column 17, lines 10-15, 45-49]*;

a controller *[Fig. 1, component 255]* for issuing one of a plurality of instructions to said associative memory device *[column 4, lines 10-19]*;

a clock device *[Fig. 1, component 256]* for outputting a synchronizing clock signal comprised of a predetermined number of clock cycles per second, said clock device outputting said synchronizing clock signal to said associative memory device and said controller *[column 4, lines 7-14]*; and

wherein said controller globally communicates one of said plurality of instructions to all of said n-cells simultaneously, within one of said clock cycles *[column 5, lines 31-49]*.

11. Referring to claim 23, Stefan has taught the data processing system of claim 22, further comprising:

a classification device *[transcoders; Fig. 12, components 39 & 40]* for selectively operating in association with a local state *[marked state]* of each of said n-cells *[column 18, lines 28-35, 45-50]*; and

wherein one of said plurality of instructions is executed by selected cells within said associative memory device in dependence upon said local state of said n-cells as directed by said classification device *[column 16, lines 44-60]*, said execution of said

instruction occurring simultaneously in each of said selected cells within one of said clock cycles *[column 5, lines 31-36]*.

12. Referring to claim 24, Stefan has taught the data processing system of claim 23, wherein: each of said n-cells include a state field *[marker field]* and a data field *[symbol field]*, said state field comprising a marker bit for encoding a local state of each of said n-cells, thereby indicating one of a marked state and a non-marked state of each of said n-cells *[column 3, lines 60-67; column 17, lines 10-15]*.

13. Referring to claim 25, Stefan has taught the data processing system of claim 24, wherein: one of said plurality of instructions issued by said controller is a `load line immediate` command *["write-all"]* whereby the contents of all of said n-cells in said marked state are replaced with data indicated by said `load line immediate` command *[column 8, lines 53-58]*.

14. Referring to claim 28, Stefan has taught the data processing system of claim 24, wherein: one of said plurality of instructions issued by said controller is a `left limit` command *["set-limit"]* whereby a left limit of a search space is set to a leftmost cell of said n-cells in said marked state *[column 11, lines 1-6]*.

15. Referring to claim 30, Stefan has taught the data processing system of claim 24, wherein: said controller may dynamically limit a search space within said n-cells *[column 10, lines 54-67]*.

16. Referring to claim 31, Stefan has taught the data processing system of claim 24, wherein: one of said plurality of instructions issued by said controller is a `find` command whereby each of said n-cells holding values equal to an argument indicated

by said `find` command is identified; and wherein said `find` command sets said marker bit to said marked state in each of said n-cells located to the right of said identified n-cells, and sets said marker bit to said non-marked state in all other of said n-cells *[column 6, lines 36-64].*

17. Referring to claim 32, Stefan has taught the data processing system of claim 24, wherein: one of said plurality of instructions issued by said controller is a `match` command *["c-find"]* whereby each of said n-cells having a marker bit in said marked state and having said data field matching an argument indicated by said `match` command *["c-find"]*, is identified; and wherein said `match` command sets said marker bit to said marked state in each of said n-cells following said identified n-cells, and sets said marker bit to said non-marked state in all other of said n-cells *[column 6, line 65 – column 7, line 22].*

18. Referring to claim 33, Stefan has taught the data processing system of claim 24, wherein: one of said plurality of instructions issued by said controller is a `find and mark left` command *["Reverse-find"]* whereby each of said n-cells holding values equal to an argument indicated by said `find and left mark` command is identified; and wherein said 'find and mark left` command *["Reverse-find"]* sets said marker bit to said marked state in each of said n-cells located to the left of said identified n-cells, and sets said marker bit to said non-marked state in all other of said n-cells *[column 10, lines 22-27].*

19. Referring to claim 34, Stefan has taught the data processing system of claim 24, wherein: one of said plurality of instructions issued by said controller is a `match and mark left` command *["Reverse-cfind"]* whereby each of said n-cells having a marker bit

in said marked state and having said data field matching an argument indicated by said `match and mark left` command *["Reverse-cfind"]*, is identified; and wherein said `match` command sets said marker bit to said marked state in each of said n-cells located to the left of said identified n-cells *[column 10, lines 28-35]*.

20. Referring to claim 38, Stefan has taught the data processing system of claim 24, wherein: one of said plurality of instructions issued by said controller is a `clr` command *["jump"]* whereby said marker bit of each of said n-cells containing a value equal to an argument indicated by said `clr` command *["jump"]* is set to said non-marked state *[column 9, lines 4-14]*.

21. Referring to claim 43, Stefan has taught the data processing system of claim 24, wherein: one of said plurality of instructions issued by said controller is a `left` command *["delete"]* whereby all of said marker bits for said n-cells are shifted leftward by one *[column 8, lines 15-25]*.

22. Referring to claim 44, Stefan has taught the data processing system of claim 24, wherein: one of said plurality of instructions issued by said controller is a `right` command *["insert"]* whereby all of said marker bits for said n-cells are shifted rightward by one *[column 7, line 65 – column 8, line 14]*.

23. Referring to claim 47, Stefan has taught the data processing system of claim 24, wherein: one of said plurality of instructions issued by said controller is a `nop` command *["set-limit-address"]* whereby no operation is executed *[column 11, lines 7-10]*.

24. Referring to claim 51, Stefan has taught the data processing system of claim 24, wherein: one of said plurality of instructions issued by said controller is a `set` command *["write-one"]* whereby a value indicated by said `set` command *["write-one"]* is stored in a leftmost of said n-cells in said marked state *[column 8, lines 48-52]*.

25. Referring to claim 52, Stefan has taught the data processing system of claim 24, wherein: one of said plurality of instructions issued by said controller is a `setall` command *["write-all"]* whereby a value indicated by said `setall` command *["write-all"]* is stored in all of said n-cells in said marked state *[column 8, lines 53-58]*.

26. Referring to claim 59, Stefan has taught the data processing system of claim 24, wherein: one of said plurality of instructions issued by said controller is a `ld` command *["write-all"]* whereby a value indicated by said `ld` command *["write-all"]* is loaded into said data field in all of said n-cells in said marked state *[column 8, lines 53-58]*.

27. Referring to claim 78, Stefan has taught the data processing system of claim 22, wherein:

said classification device *[transcoders; Fig. 12, components 39 & 40]* determines a global state *[Line-in [1] state]* of each of said n-cells *[column 16, lines 44-60]*; and

wherein said one of said plurality of instructions is executed by selected cells within said associative memory device in dependence upon both said local state *[marked state]* and said global state *[Line-in [1] state]* of said n-cells *[column 16, lines 44-60]*, said execution of said instruction occurring simultaneously in each of said selected cells within one of said clock cycles *[column 5, lines 31-36]*.

28. Referring to claim 79, Stefan has taught the data processing system of claim 22, wherein: said associative memory device allows the use of variable-length key fields *[the connex memory allows the use of variable-length character strings (i.e. key fields); column 4, lines 20-30]*.

29. Referring to claim 80, Stefan has taught the data processing system of claim 78, wherein:

said variable-length key fields include a data field and a key field, each of said n-cells having said data field and said key field *[column 4, lines 20-30]*; and

wherein data stored in each of said n-cells is alternatively considered as part of said data field and said key field at different times during execution of one of said plurality of instructions *[column 4, lines 20-30]*.

30. Referring to claim 81, Stefan has taught a method of processing data, said method comprising the steps of:

forming an associative memory device *[connex memory; Fig. 2, component 206]* to contain n-cells *[column 4, lines 20-41]*;

configuring each of said n-cells to include a processing circuit *[comparator; Fig. 14, component 55; column 17, lines 10-15, 45-49]*;

issuing one of a plurality of instructions from a controller *[Fig. 1, component 255]* to said associative memory device *[column 4, lines 10-19]*;

utilizing a clock device *[Fig. 1, component 256]* for outputting a synchronizing clock signal comprised of a predetermined number of clock cycles per second, said

clock device outputting said synchronizing clock signal to said associative memory device and said controller *[column 4, lines 7-14]*; and

globally communicating one of said plurality of instructions from said controller to all of said n-cells simultaneously, within one of said clock cycles *[column 5, lines 31-49]*.

31. Referring to claim 82, Stefan has taught a data processing system, said data processing system comprising:

a memory device *[connex memory; Fig. 2, component 206]* containing n-cells *[column 4, lines 20-41]*, each of said n-cells including a processing circuit *[comparator; Fig. 14, component 55; column 17, lines 10-15, 45-49]*;

a controller *[Fig. 1, component 255]* for issuing one of a plurality of instructions to said associative memory device *[column 4, lines 10-19]*;

a clock device *[Fig. 1, component 256]* for outputting a synchronizing clock signal comprised of a predetermined number of clock cycles per second, said clock device outputting said synchronizing clock signal to said associative memory device and said controller *[column 4, lines 7-14]*; and

wherein said controller globally communicates one of said plurality of instructions to all of said n-cells simultaneously, within one of said clock cycles *[column 5, lines 31-49]*.

Allowable Subject Matter

32. Claims 26, 27, 29, 35-37, 39-42, 45, 46, 48-50, 53-58, and 60-77 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in

independent form including all of the limitations of the base claim and any intervening claims.

33. The following is a statement of reasons for the indication of allowable subject matter: Claims 26, 27, 29, 35-37, 39-42, 45, 46, 48-50, 53-58, and 60-77 are directed towards particular instructions issued by the claimed data processing system. The instructions as claimed have not been found in the prior art and would not have been obvious as the instructions are unique to the architecture of Applicant's data processing system.

Conclusion

34. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

35. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Stefan et al., "The Connex Engine: An in-memory device for fast string operations", teaches an associative memory device containing a number of cells, each including a processing circuit and memory.

Dieffenderfer et al., U.S. Patent No. 5,822,608, teaches a processor array wherein each processor element includes an associative memory and an associated state field.

Gifford, U.S. Patent No. 4,873,626, teaches a processor array wherein each processor element includes a memory and an associated state field.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Benjamin P. Geib whose telephone number is (571) 272-8628. The examiner can normally be reached on Mon-Fri 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz Fleming can be reached on (571) 272-4145. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Benjamin P Geib
Examiner
Art Unit 2181

FRITZ FLEMING
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

10/27/2006